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1448A/PTO

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Sheet	1	of	3
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<b>Application Number</b>	<b>10/789,810</b>
<b>Filing Date</b>	<b>02/27/2004</b>
<b>First Named Inventor</b>	<b>Evgueni Goldberg</b>
<b>Art Unit</b>	<b>2129</b>
<b>Examiner Name</b>	<b>Omar F. Fernandez Rivas</b>
<b>Attorney Docket Number</b>	<b>CA7031042001</b>

[illegible][illegible]

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 2 of 3

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Application Number	10789,810
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Examiner Name	Omar F. Fernandez Rivas
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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
OFR	2	BAPTISTA, L. et al.; "The Interplay of Randomization and Learning of Real-World Instances of Satisfiability"; Proceedings of the AAAI Workshop on Leveraging Probability and Uncertainty in Computation; July 2000.	
OFR	3	BAYARDO, R. et al.; "Using CSP Look-Back Techniques to Solve Real-World SAT Instances"; Proceedings of the Fourteenth National Conference on Artificial Intelligence and Ninth Innovative Applications of Artificial Intelligence Conference; 1997; pp. 203-208; American Association for Artificial Intelligence Press; USA.	
OFR	4	BEN-SASSON, E. et al.; "Near-Optimal Separation of Tree-like and General Resolution"; Electronic Colloquium on Computational Complexity, Report No. 5; Third Workshop on the Satisfiability Problem - May 2000; January 17, 2000; pp. 14 - 18; ECCC; Israel.	
OFR	5	BIERE, A., et al.; "Symbolic Model Checking Using SAT Procedures Instead of BDDs"; Proceedings of Design Automation Conference - DAC'99; 1999; pp. 317 - 320; ACM; USA.	
OFR	6	BRAYTON, R.K., et al.; "Logic Minimization Algorithms for VLSI Synthesis"; Kluwer Academic Publishers, 1984; USA.	
OFR	7	BURCH, J. R., et al.; "Tight Integration of Combination Verification Methods"; Proceedings of the International Conference on Computer-Aided Design; 1998; pp. 570 - 576; ACM, USA.	
OFR	8	DAVIS, M., et al.; "A Machine Program for Theorem-Proving"; Communications of the ACM; 1962; pp. 394 - 397; USA.	
OFR	9	DUBOIS, O., et al.; "SAT versus UNSAT"; Second DIMACS Series in Discrete Mathematics and Theoretical Computer Science; 1996; pp. 415 - 436; Volume 26; American Mathematical Society.	
OFR	10	FREEMAN, J.W.; "Improvements to Propositional Satisfiability Search Algorithms"; A Dissertation in Computer and Information Science, University of Pennsylvania, 1995; 1995; USA.	
OFR	11	GOLDBERG, E. et al.; "Using SAT for Combinational Equivalence Checking"; Proceedings of the Design Automation and Test in Europe Conference - 2001; 2001; pp. 114 - 121; IEEE; USA.	
OFR	12	GOMES, C. P., et al.; "Boosting Combinatorial Search Through Randomization"; Proceedings of the International Conference on Principles and Practice of Constraint Programming; 1998; pp. 431 - 437; American Association for Artificial Intelligence Press/ The MIT Press; USA.	
OFR	13	GOMES, C. P., et al.; "Heavy-Tailed Distributions in Combinatorial Search"; Principles and Practice of Constraint Programming - CP97; 1997; pp. 121 - 135; Springer.	
OFR	14	LI, C. M.; "A Constraint-Based Approach to Narrow Search Trees for Satisfiability"; Information Processing Letters 71; 1999; pp. 75 - 80; Volume 71; Elsevier Science B.V.; France.	
Examiner Signature	/Omar Fernandez Rivas/		Date Considered 12/20/2006

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OFR	15	MARQUES-SILVA, J.; "The Impact of Branching Heuristics in Propositional Satisfiability Algorithms"; Proceedings of the 9th Portuguese Conference on Artificial Intelligence (EPIA); September 1999; LNAI; pp. 62 - 74; 1695; Portugal.	
OFR	16	MARQUES-SILVA, J. P. et al.; "GRASP: A New Search Algorithm for Satisfiability"; CSE-TR-292-96; April 10, 1996; pp. 1 - 17; The University of Michigan; USA.	
OFR	17	MARQUES-SILVA, J. P. et al.; "GRASP: A Search Algorithm for Propositional Satisfiability"; IEEE Transactions on Computers; May 1999; pp. 506- 521; Volume 48; No. 5.	
OFR	18	MOSKEWICZ, M. W. et al.; "Chaff: Engineering an Efficient SAT Solver"; Proceedings of the 38th Design Automation Conference -DAC '01; 2001; pp. 530 - 535; ACM; USA.	
OFR	19	NOVIKOV, Y. A.; "Using Restarts When Solving SAT-Instances"; Proceedings of the Fourth International Conference on Computer-Aided Design of Discrete Devices CAD DD '01; 2001; pp. 166 - 174; Volume 3; National Academy of Sciences of Belarus Institute of Engineering Cybernetics; Republic of Belarus.	
OFR	20	STEPHAN, P., et al.; "Combinational Test Generation Using Satisfiability"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; September 1996; pp. 1167 -1176; Volume 15; Number 9; IEEE; USA.	
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OFR	22	ZHANG, H.; "SATO: An Efficient Propositional Prover"; Proceedings of the 14th International Conference on Automated Deduction - CADE- 14; July 1997; pp. 272 - 275; Springer; Australia.	
OFR	23	SATLIB - Benchmark Problems; 2004; <a href="http://www.satlib.org/benchm.html">http://www.satlib.org/benchm.html</a> .	
OFR	24	The SAT-Ex site; 2004; <a href="http://www.lri.fr/~simon/satex/satex.php3">http://www.lri.fr/~simon/satex/satex.php3</a> .	
Examiner Signature	/Omar Fernandez Rivas/		Date Considered
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